WHAT IS CLAIMED IS

1. A semiconductor device having a wiring pattern that is formed by etching a conductive layer using a resist pattern as a mask, the semiconductor device comprising:

a contact section formed in an interlayer dielectric layer;

a first wiring formed over the interlayer dielectric layer and disposed with a separation from the contact section shorter than a specified separation; and

a second wiring having a connection region to be connected to the contact section,

wherein the second wiring has an extension section extending in a non-wiring region in the connection region to be connected to the contact section, and

the extension section is disposed in at least one section of the connection region other than sides thereof facing the first wiring.

2. A semiconductor device according to claim 1, wherein the separation shorter than a specified separation is a minimum separation between wirings in the wiring pattern.

3. A semiconductor device according to claim 1, wherein the connection region is square in its plan configuration having generally an identical diameter of the contact section, or square in its plan configuration having a diameter greater than that of the contact section.

4. A semiconductor device according to claim 1, wherein the extension section has an identical width as a width of the wiring.

5. A semiconductor device according to claim 1, wherein the extension section has an extension length identical with the width of the wiring.

6. A semiconductor device according to claim 1, wherein the extension section is square in its plan configuration.

7. A semiconductor device having a wiring pattern formed by etching a conductive layer using a resist pattern as a mask, the semiconductor device comprising:

a contact section formed over an interlayer dielectric layer;

a first wiring formed over the interlayer dielectric layer and disposed with a minimum inter-wiring separation with respect to the contact section; and

a second wiring having a connection region to be connected to the contact section and extending in parallel with the first wiring,

wherein the connection region of the second wiring has a generally square plan configuration,

the second wiring has an extension section extending in a non-wiring region in the connection region, and

the extension section is disposed on sides of the connection region other than sides thereof facing the first wiring.

8. A semiconductor device having a wiring pattern formed by etching a conductive layer using a resist pattern as a mask, the semiconductor device comprising:

a contact section formed in an interlayer dielectric layer;

a first wiring formed over the interlayer dielectric layer and disposed with a minimum inter-wiring separation with respect to the contact section; and

a second wiring having a connection region to be connected to the contact section and extending in a direction perpendicular to the first wiring,

wherein the connection region of the second wiring has a generally square plan configuration,

the second wiring has an extension section extending in a non-wiring region in the connection region, and

the extension section is disposed in sides of the connection region other than sides thereof facing the first wiring.

9. A semiconductor device having a wiring pattern formed by etching a conductive layer using a resist pattern as a mask, the semiconductor device comprising:

a contact section formed in an interlayer dielectric layer;

a first wiring formed over the interlayer dielectric layer and disposed with a minimum inter-wiring separation with respect to the contact section; and

a second wiring having a connection region to be connected to the contact section and having a section extending in parallel with the first wiring and a section extending in a direction perpendicular to the first wiring,

wherein the connection region of the second wiring has a generally square plan configuration,

the second wiring has an extension section extending in a non-wiring region in the connection region, and

the extension section is disposed on sides of the connection region other than sides thereof facing the first wiring.

10. A semiconductor device having a wiring pattern formed by etching a conductive layer using a resist pattern as a mask, the semiconductor device comprising:

a contact section formed in an interlayer dielectric layer;

a first wiring formed over the interlayer dielectric layer and disposed with a minimum inter-wiring separation with respect to the contact section; and

a second wiring having only a connection region to be connected to the contact section,

wherein the connection region of the second wiring has a generally square plan configuration,

the second wiring has an extension section extending in a non-wiring region in the connection region; and

the extension section is disposed on sides of the connection region other than sides thereof facing the first wiring.

11. A semiconductor device having a wiring pattern formed by etching a conductive layer using a resist pattern as a mask, the semiconductor device comprising:

a contact section formed in an interlayer dielectric layer;

a plurality of first wirings formed over the interlayer dielectric layer and disposed with a minimum inter-wiring separation with respect to the contact section; and

a second wiring having at least one connection region to be connected to the contact section,

wherein the connection region of the second wiring has a generally square plan configuration,

the second wiring has an extension section extending in a non-wiring region in the connection region, and

the extension section is disposed on sides of the connection region other than sides thereof facing the plurality of first wirings.

12. A semiconductor device having a wiring pattern formed by etching a conductive layer using a resist pattern as a mask, the semiconductor device comprising:

a contact section formed in an interlayer dielectric layer; and

a wiring having a connection region to be connected to the contact section,

wherein the connection region of the wiring has a generally square plan configuration, and

the wiring has an extension section extending in a non-wiring region in the connection region.

13. A semiconductor device according to claim 12, wherein the wiring is in a line-like shape and has extension sections on three sides of the connection region.

14. A semiconductor device according to claim 12, wherein the wiring is formed from the connection region and have extension sections on four sides of the connection region.

15. A method for manufacturing a semiconductor device, the method comprising:

a first step of forming a mask pattern by disposing line patterns, setting a connection region pattern that at least covers a connection hole pattern in a lower layer, disposing extension patterns on sides of the connection region pattern, and erasing those of the extension patterns that face the line patterns with a separation shorter than a specified separation between the sides of the connection region pattern and adjacent ones of the line patterns;

a second step of forming a resist pattern on a conductive layer by lithography using the mask pattern; and

a third step of forming wiring patterns by etching the conductive layer using the resist pattern as a mask.

16. A method for manufacturing a semiconductor device according to claim 15, wherein the separation shorter than a specified separation is a minimum separation between lines in the line patterns.

17. A method for manufacturing a semiconductor device according to claim 15, wherein the connection region pattern is square having generally an identical size of the connection hole pattern, or square having a size greater than that of the connection hole pattern.

18. A method for manufacturing a semiconductor device according to claim 15, wherein the extension pattern has a width identical with a width of a line in the line patterns.

19. A method for manufacturing a semiconductor device according to claim 15, wherein the extension pattern has an extension length identical with a width of a line in the line patterns.

20. A method for manufacturing a semiconductor device according to claim 15, wherein the extension pattern is square.

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